What is claimed is:

1. A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, said semiconductor device comprising:

a plurality of device formation regions in which predetermined devices are to be formed respectively, said plurality of device formation regions being provided in said SOI layer;

at least one isolation region provided in said SOI layer for insulatively isolating said plurality of device formation regions from each other; and

a body region provided in said SOI layer and capable of externally fixing electric potential,

wherein at least part of said at least one isolation region includes a partial isolation region having a partial insulation region formed in an upper part thereof and a semiconductor region formed in a lower part thereof, said semiconductor region serving as part of said SOI layer and being formed in contact with at least one of said plurality of device formation regions and said body region.

2. The semiconductor device according to claim 1,

wherein said plurality of device formation regions include a plurality of first device formation regions for a first device, and a plurality of second device formation regions for a second device; said at least one isolation region further includes a complete isolation region having a complete insulation region extending through said SOI layer; and said partial isolation region includes first and second partial isolation regions, and

wherein said plurality of first device formation regions are isolated from each

other by said first partial isolation region, said plurality of second device formation regions are isolated from each other by said second partial isolation region, and said plurality of first device formation regions and said plurality of second device formation regions are isolated from each other by said complete isolation region.

3. The semiconductor device according to claim 1,

wherein said plurality of device formation regions include a plurality of device formation regions for a first circuit and a plurality of device formation regions for a second circuit, and

wherein said plurality of device formation regions for said first circuit are isolated from each other by a complete isolation region extending through said SOI layer, and said plurality of device formation regions for said second circuit are isolated from each other by said partial isolation region.

4. The semiconductor device according to claim 1,

wherein said plurality of device formation regions include a device formation region for a predetermined circuit, and a device formation region for a circuit other than said predetermined circuit, and

wherein said device formation region for said predetermined circuit and said device formation region for said circuit other than said predetermined circuit are isolated from each other by a complete isolation region extending through said SOI layer.

5. The semiconductor device according to claim 1,

wherein said at least one isolation region includes a plurality of isolation regions, and at least one of said plurality of isolation regions has a predetermined width

and extends substantially perpendicularly to a surface of said semiconductor substrate.

6. A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, said semiconductor device comprising:

a plurality of device formation regions in which predetermined devices are to be formed respectively, said plurality of device formation regions being provided in said SOI layer;

at least one isolation region provided in said SOI layer for insulatively isolating said plurality of device formation regions from each other; and

a body region capable of externally fixing electric potential,

wherein said body region is formed in contact with one of top and bottom surfaces of at least one of said plurality of device formation regions.

7. The semiconductor device according to claim 1,

wherein at least part of said at least one isolation region further comprises a combined isolation region including said partial isolation region and a complete insulation region extending through said SOI layer, said partial isolation region and said complete insulation region being continuous with each other.

8. The semiconductor device according to claim 7,

wherein said partial isolation region has a flat and even top surface.

9. The semiconductor device according to claim 7,

wherein said semiconductor region of said combined isolation region has a

thickness which is not greater than one-half the thickness of said SOI layer.

10. The semiconductor device according to claim 7,

wherein said complete insulation region of said combined isolation region has a width which is not greater than one-half the width of said combined isolation region.

11. The semiconductor device according to claim 1,

wherein said at least one isolation region further includes a complete isolation region having a complete insulation region extending through said SOI layer,

wherein said plurality of device formation regions include an input/output NMOS transistor formation region and an input/output PMOS transistor formation region which are disposed adjacent to each other, and

wherein said complete isolation region is formed at least in the vicinity of a boundary between said input/output NMOS transistor formation region and said input/output PMOS transistor formation region.

12. The semiconductor device according to claim 11,

wherein said plurality of device formation regions further include an internal circuit formation region disposed adjacent to one of said input/output NMOS transistor formation region and said input/output PMOS transistor formation region, and

wherein said complete isolation region is further formed in the vicinity of a boundary between said internal circuit formation region and one of said input/output NMOS transistor formation region and said input/output PMOS transistor formation region which is disposed adjacent to said internal circuit formation region.

13. The semiconductor device according to claim 1,

wherein said at least one isolation region further includes a complete isolation region having a complete insulation region extending through said SOI layer,

wherein said plurality of device formation regions include an NMOS transistor formation region and a PMOS transistor formation region which are disposed adjacent to each other,

wherein said complete isolation region is formed in a complete isolation region formation location situated within said PMOS transistor formation region in the vicinity of a boundary between said NMOS transistor formation region and said PMOS transistor formation region, and

wherein said partial isolation region surrounds said NMOS transistor formation region and said PMOS transistor formation region except in said complete isolation region formation location.

14. The semiconductor device according to claim 1,

wherein said plurality of device formation regions include a transistor formation region of a first conductivity type,

wherein said partial isolation region includes a peripheral partial isolation region surrounding said transistor formation region, and

wherein said body region includes a peripheral body region of a second conductivity type surrounding said peripheral partial isolation region.

15. The semiconductor device according to claim 1,

wherein said plurality of device formation regions include a MOS transistor formation region, and

wherein said body region includes an adjacent-to-source body region disposed adjacent to a source region of said MOS transistor formation region,

said semiconductor device further comprising

an electric potential setting region commonly connected to said source region and said adjacent-to-source body region.

16. The semiconductor device according to claim 1,

wherein said semiconductor region of said partial isolation region includes first and second partial semiconductor regions, and

wherein the impurity concentration of said first partial semiconductor region is higher than that of said second partial semiconductor region.

17. The semiconductor device according to claim 1,

wherein said plurality of device formation regions include a MOS transistor formation region of a first conductivity type, and said semiconductor region of said partial isolation region includes a region of a second conductivity type, and

wherein a peak of the impurity concentration of said semiconductor region of said partial isolation region is deeper from a surface of said SOI layer than a peak of the impurity concentration of a drain/source region formed in contact with said semiconductor region in said MOS transistor formation region.

18. The semiconductor device according to claim 1,

wherein said plurality of device formation regions include a MOS transistor formation region, and

wherein a peak of the impurity concentration of a channel formation region of

said MOS transistor formation region is deeper from a surface of said SOI layer than a peak of the impurity concentration of said semiconductor region of said partial isolation region.

19. The semiconductor device according to claim 1,

wherein said partial isolation region has a surface corner part and a bottom corner part, said bottom corner part having a radius of curvature greater than that of said surface corner part.

20. The semiconductor device according to claim 7,

wherein said partial insulation region of said combined isolation region has a bottom corner part and a stepped part defined between said complete insulation region and said partial insulation region, said stepped part having a radius of curvature less than that of said bottom corner part.

21. The semiconductor device according to claim 1,

wherein said at least one isolation region further includes a complete isolation region having a complete insulation region extending through said SOI layer,

said semiconductor device further comprising

an inductance element formed in an inductance formation region lying in an upper part of said SOI layer,

wherein said complete isolation region is formed under said inductance formation region.

22. The semiconductor device according to claim 1,

wherein said plurality of device formation regions include a MOS transistor formation region, and said body region includes a gate-connected body region electrically connected to a gate electrode of a MOS transistor formed in said MOS transistor formation region, and

wherein said partial isolation region surrounds said MOS transistor formation region.

23. A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, said semiconductor device comprising:

a device formation region in which a predetermined device is to be formed, said device formation region being provided in said SOI layer; and

a peripheral isolation region provided in said SOI layer and surrounding said device formation region, said peripheral isolation region including a partial isolation region having a partial insulation region formed in an upper part thereof and a semiconductor region formed in a lower part thereof and serving as part of said SOI layer,

wherein said semiconductor region is formed in contact with said device formation region and is floating.